Patent

Customer No.: 31561
Docket No. 11870-US-PA
Application No.: 10/707,867

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Applicant : Yao-Chi Wang
Application No. : 10/707,867
Filed : January 20, 2004
For : AUTOMATIC THRESHOLD VOLTAGE CONTROL CIRCUIT AND SIGNAL CONVERTING CIRCUIT AND METHOD THEREOF
Art Unit : 2819
Examiner : Nguyen, Linh V.

TRANSMITTAL LETTER

002-1-571-273-8300
(Via fax: 1+16 pages)

Assistant Commissioner for Patent
Alexandria, VA 22314

In response to the Notice of Appeal filed on July 5, 2005, please find the *Appeal Brief* in 16 pages.

Please charge the payment in the amount of US$500 to account No. 50-2620 (Order No.: 11870-US-PA) to cover the fee set forth in 37 CFR 1.17(c) for filing an Appeal Brief.

If the payment is not fully covered in response thereof, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No.: 50-2620 (Order No.: 11870-US-PA).

Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

Date: September 2, 2005 By: Belinda Lee
Belinda Lee
Registration No.: 46,863

Please send future correspondence to:
7F. -1, No. 100, Roosevelt Rd.,
Sec. 2, Taipei 100, Taiwan, R.O.C.
Tel: 886-2-2369 2800 Fax: 886-2-2369 7233 / 886-2-2369 7234
E-MAIL: BELINDA@JCIPGroup.com.tw; USA@JCIPGroup.com.tw

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE WANG, Yao-Chi

Application for Patent

Filed January 20, 2004

Serial No. 10/707,867

FOR:
AUTOMATIC THRESHOLD VOLTAGE CONTROL CIRCUIT AND SIGNAL CONVERTING CIRCUIT AND METHOD THEREOF

APPEAL BRIEF

JIANQ CHYUN INTELLECTUAL
PROPERTY OFFICE.
Attorneys for Applicants

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is Sunplus Technology Co., Ltd., the assignee of record.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals and/or interferences.

III. STATUS OF THE CLAIMS

A total of 20 claims were presented during prosecution of this application. Applicant appeals rejected claims 1-20.

IV. STATUS OF THE AMENDMENTS

Claims 1-20 are pending, have been finally rejected, and this appeal is taken from the Examiner's final rejection of claims 1-20.

V. SUMMARY OF THE INVENTION

As for example shown in FIG. 3, the first capacitor C2 is associated with the threshold voltage V_{REF}. A clock generator 320 is for generating a plurality of clock signals. A switching capacitor network 330 is coupled to the first capacitor C2, wherein the switching capacitor network 330 receives an analog signal Vin and the clock signals from the clock generator 320, so as to ***store a portion of charges of the analog signal***, and outputs the portion of charges according to the clock signals, and generates a threshold voltage V_{REF} associated with the first capacitor C2.

It should be noted that, due to the control from the clock signal, the switching capacitor network 330 only stores a portion of charges of the input analog signal Vin for producing the threshold voltage V_{REF} at the first capacitor C2. Basically, this circuit can also operate like a RC filter.

Further, in order to achieve the ADC circuit, the comparator 310 is used. The comparator compares the threshold voltage V_{REF} and the input analog signal Vin, so as to get the digital signal.

VI. ISSUES

A. *Were claims 1-4 and 7-9 properly rejected under 35 U.S.C. 102(b) as being anticipated by Kusumoto et al.?*

B. *Were claims 10, 11 and 16-19 properly rejected under 35 U.S.C. 102(b) as being anticipated by Zhou et al.?*

C. *Were claims 5 and 6 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Kusumoto et al. in view of Zhou et al.?*

D. *Were claims 12-15 and 20 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. in view of Kusumoto et al.?*

VII. GROUPING OF THE CLAIMS

Applicant proposes two groups of claims to stand or fall together. The first group includes claims 1-9 ("Group I"). The second group includes claims 10-20 ("Group II").

Group II is based on Group I. However, the additional comparator is used, so as to achieve the ADC circuit.

VIII. ARGUMENTS

A. The related law

The standard for lack of novelty (i.e. anticipation) is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements. *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 U.S.P.Q. 81, 90 (Fed. Cir. 1986).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

For a prior art refcrence to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. ..... These elements must be arranged as in the claim under review, ... but this is not an 'ipsissimis verbis' test. *In re Bond*, 910, F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The inquiry as to anticipation is symmetrical with the inquiry as to infringement of a patent. A classic test of anticipation provides : That which will infringe, if later, will anticipate, if earlier. *Knapp v. Morss*, 150 U.S. 221, 37 L. Ed. 1059, 14 S. Ct. 81 (1893); *Lindermann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1459, 221 U.S.P.Q. 481 (Fed. Cir. 1984). Therefore, by analogy, the all elements rule used for a determination of infringement finds its applicability in a determination of anticipation. Discussion of the all elements rule can be found in *Becton Dickinson and Co. v. C.R. Bard Inc.*, 17 U.S.P.Q. 2d 1962, 1967 (Fed. Cir 1989) and *Hi-Life Products Inc. v. American National Water-Mattress Corp.*, 6 U.S.P.Q.2d 1132, 1133 (Fed. Cir. 1988).

A prima facie case of obviousness requires that the reference teachings "appear to have suggested the claimed subject matter." *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143, 147 (CCPA 1976). To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." *In re Lalu*, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984). There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

Finally, if an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d, 1596 (Fed. Cir. 1988).

B. Claims 1-4 and 7-9 were improperly rejected under 35 U.S.C. 102(b) as being anticipated by Kusumoto et al.

1) The rejections

The Examiner rejected claims 1-4 and 7-9 under 35 U.S.C. 102(b) as being anticipated by Kusumoto et al. (U. S. Patent 6,025,794; hereinafter Kusumoto), seeing to Final Action.

2) The prior art

Kusumoto in FIG. 24 discloses a circuit using the switches 248, 249, and 2414, so as to produce the voltage Va for driving the circuit to be driven 244. Fig. 25 discloses a timing for the switches. As a result, the waveform of driving voltage Va is obtained.

For the operation in Kusumoto, the switches 248 and 249 with the capacitor C0 is used to hold a voltage while the capacitor C1 can produce the voltage level Va to the circuit to be driven 244. For the next period for transferring, the voltages held in the capacitor C0 with the capacitor C1 are transferred to the circuit 244. At the end, he driving signal (Va) with the alternating square waveform is produced for driving the circuit 244. Basically, the circuit in FIG. 24 is self-independent, and cannot be separated in consideration.

3) The prior art distinguished

(a) Group I

With respect to independent claim 1 (see FIG. 3), the clock generator generates the clock signal to control the switching capacitor network 330, so that the switching capacitor network 330 only stores a portion of charges of the input analog signal. Then, the portion of charges of the input analog signal is output according to the clock signal to server as the threshold voltage or a reference voltage V_{REF}.

Further, according to the circuit of the present invention, the switching capacitor network 330 associated with the first capacitor C2 can serve as the RC filter [0025].

In re Kusumoto, the circuit in FIG. 24 can not be separated consideration.

Also and, the clocks in Fig. 25 do not control the switches 248 and 249 to produce a threshold voltage at the line 234 with a portion of charges in the input signal as recited in independent claim 1.

Further, the clocks in Fig. 25 do not specifically cause the capacitor C0 to just store a portion of the charges from the input signal, so as to produce a threshold voltage V_{REF}, as recited in independent claim 1.

For at least the foregoing reasons, Kusumoto does not disclose the features of the present invention.

In another point of view, the capacitor C1 is coupled with the switch 2414 and the capacitor Cf together in operation. This is not equal to the first capacitor C2 of the present invention in operation to produce the threshold voltage V_{REF}.

With at least the same foregoing reasons, dependent claims 2-4 and 7-9 define over the prior art as well.

Applicant respectfully traverses the rejections for at least the reasons set forth above.

C. Claims 10, 11 and 16-19 were improperly rejected under 35 U.S.C. 102(b) as being anticipated by Zhou et al.

1) The rejections

Claims 10, 11 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhou et al. (U. S. Patent 6,124,819; hereinafter Zhou).

2) The prior art

Zhou in Fig. 6 discloses an ADC circuit and Fig. 7 discloses a set of clocks. The sample and hold capacitors 50 and 52 as a pair are used (col. 7, lines 66-67). This circuit with the pair of sample and hold capacitors 50 and 52 receives the analog signals Vs, VR, and Vref. The comparator 62 receives the signal S 82 and the rest level R 78 (col. 8, lines 38-39) ***but not receives the input signal Vs 80.***

3) The prior art distinguished

(a) Group II

In FIG. 6 of Zhou, the Final Office Action in page 6 considers the MOS transistors of 75, 80, 84, 74 as the switching capacitor network. In addition, the Final Office Action in page 7 also considers different input analog signals (Vs, VR, Vref), which are input to the transistors 75, 80, and 84, and then passes the transistor 74. The Office Action also considers the comparator 62 for receives the signal S and the reset level R. The clock signals are referred to FIG. 7.

In comparing FIG. 3 of the present invention with FIG. 6 of Zhou, clearly the two circuits are different in design circuit structure and operation mechanism. The MOS transistors of 75, 80, 84, 74 and the comparator 62 do not disclose the same ADC circuit of the present invention.

In the present invention, the comparator receives the input analog signal V_{IN} and the threshold voltage V_{REF} from the switching capacitor network 330. The switching capacitor network 330 store a portion of the input analog signal V_{IN}, so as to produce the threshold voltage V_{REF} as the input for the comparator. Zhou failed to disclose the circuit structure as recited in claim 10 and the method as recited in claim 19.

Further with respect to claim 11, claim 11 recites the structure of the switching capacitor network 330, which has at least one capacitor coupled to the connection node between two adjacent switches. Capacitor 50 with the switches in FIG. 24 of Zhou also fails to disclose the structure of the switching capacitor network 330 of the present invention.

With at least the same foregoing reasons, dependent claims 16-18 define over the prior art as well.

Applicant respectfully traverses the rejections for at least the reasons set forth above.

D. Claims 5 and 6 were improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Kusumoto et al. in view of Zhou et al.

Claims 5 and 6, in Group I, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusumoto in view of Zhou. Applicant respectfully traverses the rejections for at least the reasons set forth below.

For at least the foregoing reasons applied to independent claim 1 for Group I, dependent claims 5 and 6 are not fully disclosed by Kusumoto.

Zhou is cited in combination with Kusumoto. However, Zhou also failed to supply the missing features in independent claim 1.

Even further, Kusumoto and Zhou respectively disclose the two different types of circuits. The motivation in combination of Kusumoto and Zhou is not presented.

For at least the same foregoing reasons, dependent claims 5 and 6 should be allowabe.

E. Claims 12-15 and 20 were improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. in view of Kusumoto et al.

Claims 12-15 and 20, in Group II, are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou in view of Kusumoto. Applicant respectfully traverses the rejections for at least the reasons set forth below.

For at least the foregoing reasons applied to independent claims 10 and 19 for Group II, dependent claims 12-15 and 20 are not fully disclosed by Zhou.

Kusumoto is cited in combination with Zhou. However, Kusumoto also failed to supply the missing features in independent claims 10 and 19.

Even further, Kusumoto and Zhou respectively disclose the two different types of circuits. The motivation in combination of Kusumoto and Zhou is not presented.

For at least the same foregoing reasons, dependent claims 12-15 and 20 should be allowabe.

IX. CONCLUSION

As noted, none of the cited art, either alone or in combination, can be said to disclose or render obvious the appealed claims. The references disclose the circuits in different structures and in different operation mechanisms from the present invention. The "switching capacitor network" of the present invention is properly controlled by a clock, so as to store a portion of the charges of the input analog signal, so as to produce the associated threshold voltage. In further application, the threshold voltage and the input analog signal are compared, so as to achieve the ADC circuit. These features are not disclosed by the prior art references.

Further, the circuits disclosed by the references are in different design and operation mechanism. The motivation of combination is not presented.

Accordingly, Applicant believes that the rejections under 35 U.S.C. 102 and 103 are in error, and respectfully requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejections of the claims on appeal.

Date : September 2, 2005

Respectfully Submitted,

Belinda Lee

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw

APPENDIX A - CLAIMS ON APPEAL

1. (original) An automatic threshold voltage control circuit, comprising:

a first capacitor, having a first terminal and a second terminal, wherein said first terminal is coupled to a first voltage level;

a clock generator, for generating a plurality of clock signals; and

a switching capacitor network, coupled to said second terminal of said first capacitor, wherein the switching capacitor network receives an analog signal and said clock signals, stores a portion of charges of said analog signal, and outputs said portion of charges according to said clock signals, and generates a threshold voltage associated with said first capacitor.

2. (original) The circuit of claim 1, wherein said switching capacitor network comprises:

a plurality of sensor control switches, wherein one of said sensor control switches is controlled by said clock signals for turning on/off, said sensor control switches are series-connected to for a series structure having a first terminal and a second terminal, said first terminal of said series structure receiving said analog signal and said second terminal of series structure being coupled to said second terminal of said first capacitor to output said threshold voltage; and

at least a second capacitor, having a first terminal and a second terminal, wherein said first terminal of said second capacitor is coupled to a node connected to two adjacent sensor control switches in said series structure, said second terminal of said second capacitor is coupled to a second voltage level.

3. (original) The circuit of claim 2, wherein said of clock signals have a same frequency with different phases respectively.

4. (original) The circuit of claim 3, wherein said plurality of clock signals do not

overlap.

5. (original) The circuit of claim 4, wherein said plurality of sensor control switches are MOSFETs.

6. (original) The circuit of claim 5, wherein said first voltage level and said second voltage level are DC voltage levels.

7. (original) The circuit of claim 1, wherein said circuit applies to a frequency-shift keying communication system.

8. (original) The circuit of claim 1, wherein said circuit applies to an amplitude-shift keying communication system.

9. (original) The circuit of claim 1, wherein said circuit applies to an on/off keying communication system.

10. (original) An analog-to-digital signal converter circuit, comprising:

a first capacitor, having a first terminal and a second terminal, wherein said first terminal is coupled to a first voltage level;

a clock generator, for generating a plurality of clock signals;

a switching capacitor network, coupled to said second terminal of said first capacitor, wherein the switching capacitor network receives an analog signal and said clock signals, said switching capacitor network stores a portion of charges of said analog signal, and outputs said portion of charges according to said clock signals, and generates a threshold voltage associated with said first capacitor; and

a comparator, for comparing said threshold voltage with said analog signal and outputting a digital signal.

11. (original) The circuit of claim 10, wherein said switching capacitor network comprises:

a plurality of sensor control switches, wherein one of said sensor control switches is controlled by said clock signals for turning on/off, said sensor control switches are series-connected to form a series structure having a first terminal and a second terminal, said first terminal of said series structure receiving said analog signal and said second terminal of series structure being coupled to said second terminal of said first capacitor so as to output said threshold voltage; and

at least a second capacitor, having a first terminal and a second terminal, said first terminal of said second capacitor being coupled to a connection between two adjacent sensor control switches in said series structure, said second terminal of said second capacitor being coupled to a second voltage level.

12. (original) The circuit of claim 11, wherein said of clock signals have a same frequency with different phases respectively.

13. (original) The circuit of claim 12, wherein said clock signals do not overlap.

14. (original) The circuit of claim 13, wherein said sensor control switches are MOSFETs.

15. (original) The circuit of claim 14, wherein said first voltage level and said second voltage level are DC voltage levels.

16. (original) The circuit of claim 10, wherein said circuit applies to a frequency-shift keying communication system.

17. (original) The circuit of claim 10, wherein said circuit applies to an amplitude-shift keying communication system.

18. (original) The circuit of claim 10, wherein said circuit applies to an on/off keying communication system.

19. (original) A method for converter an analog signal to a digital signal, comprising:

providing a first capacitor and a plurality of clock signals;

storing a portion of charges of an analog signal according to said clock signals;

generating a threshold voltage according to said clock signals based on said portion of charges associated with said first capacitor ; and

comparing said threshold voltage with said analog signal in order to output a digital signal.

20. (original) The method for converter of claim 19, wherein said clock signals comprises a first clock signal and a second clock signal, said first and second clock signals have a same frequency but not overlapping, and said step of generating said threshold voltage further comprising:

providing a second capacitor;

conducting said analog signal to said second capacitor according to said first clock signal to store said portion of charges of said analog signal in said second capacitor; and

conducting said first capacitor and said second capacitor in response to said second clock signal in order to generate said threshold voltage based on said portion of charges of said analog signal associated with said first capacitor.